

FIG. 1

FIG. 2

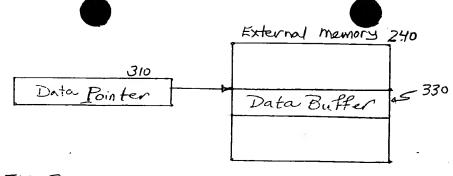


FIG. 3A

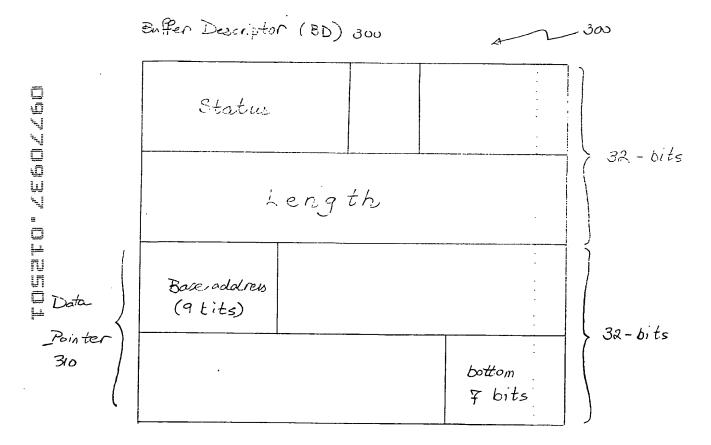


FIG.3B

Configuration	Bit 8	Bit 7		Depth
1	0	0	1-4	32-
2	0	1	1-2	40
			3-4	24
3	1	0	1	80
			2-3	24
			4	0
4	1	1	1	64
			2	64
			3	0
			4	0

Trans mit Ready Queue Configuration

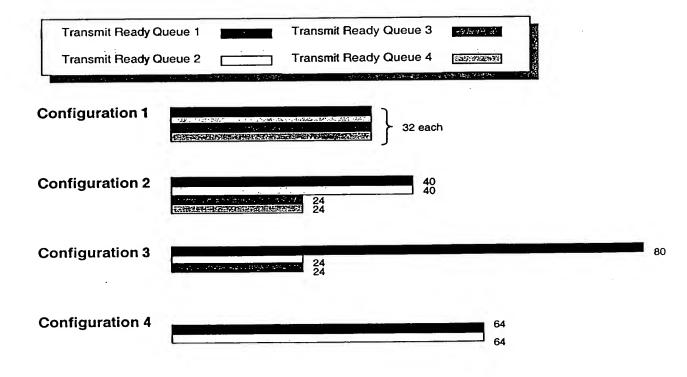


FIG. 4

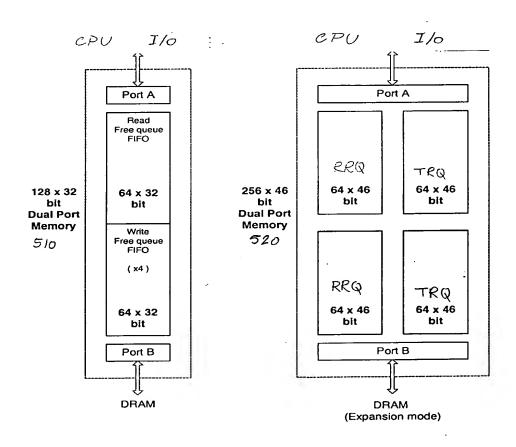
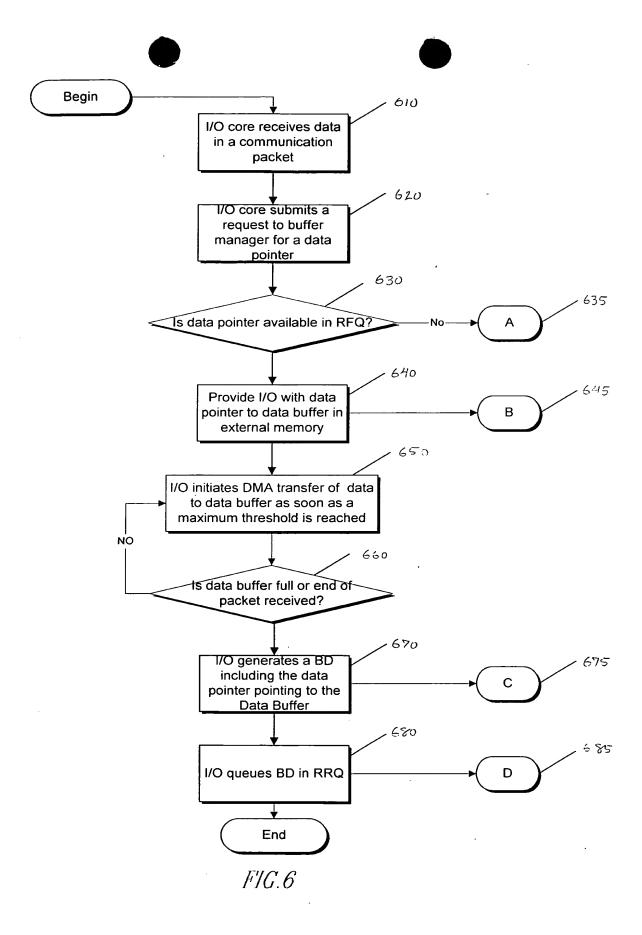


FIG. 5



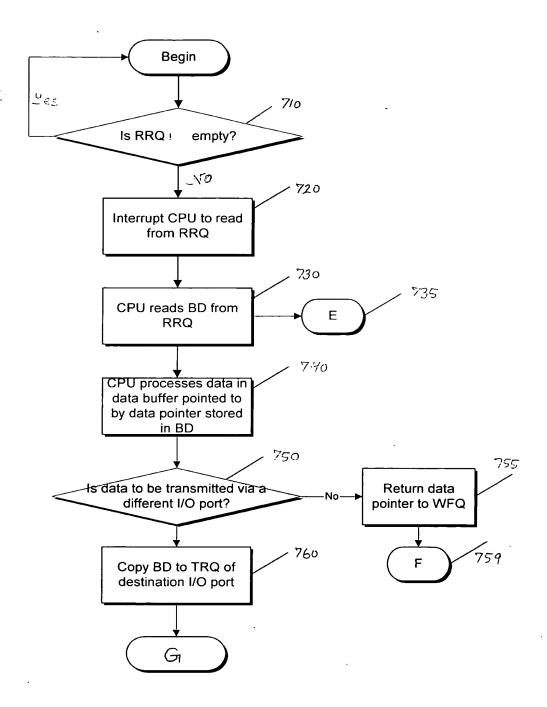
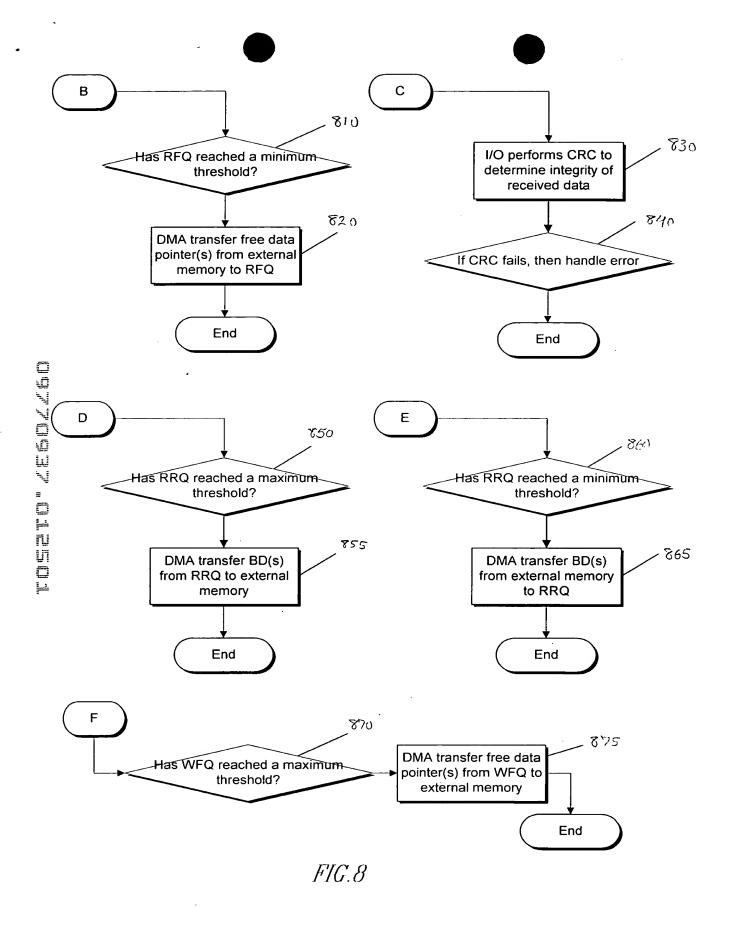
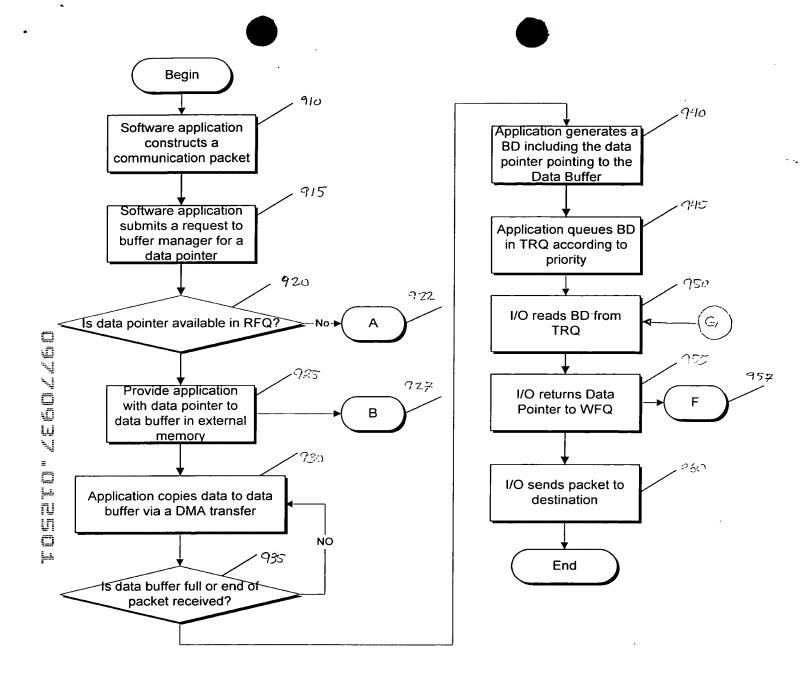
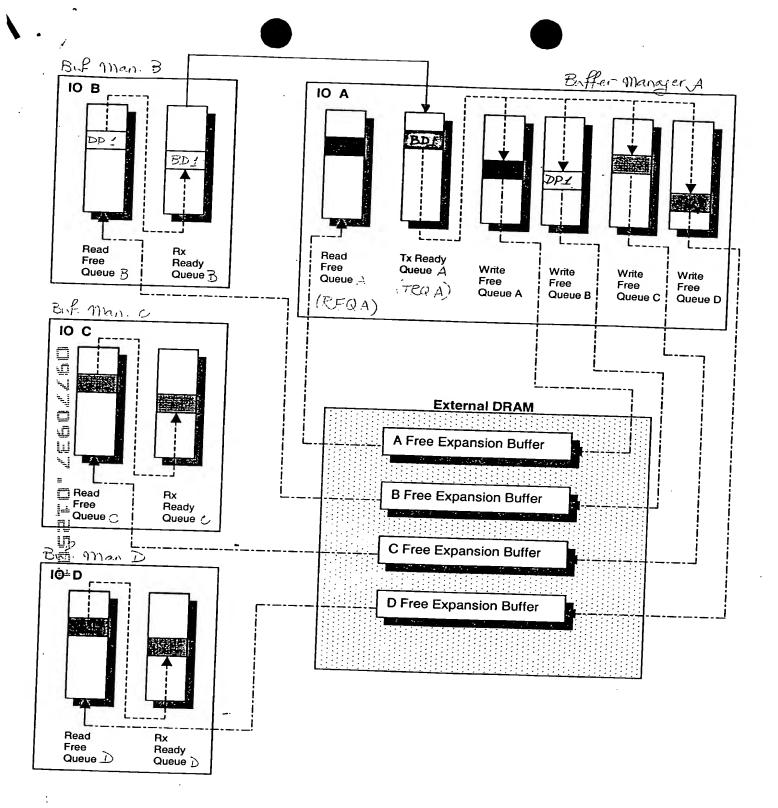


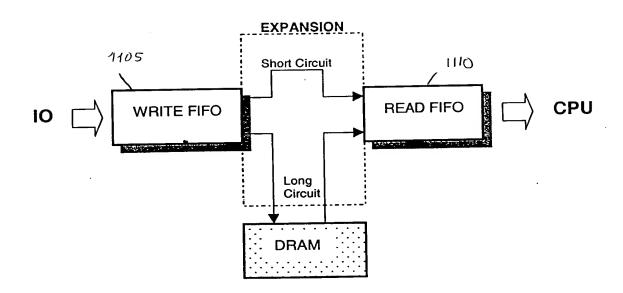
FIG. 7



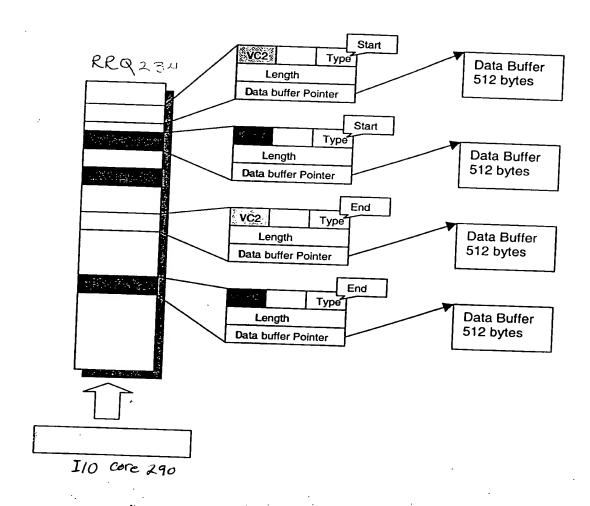




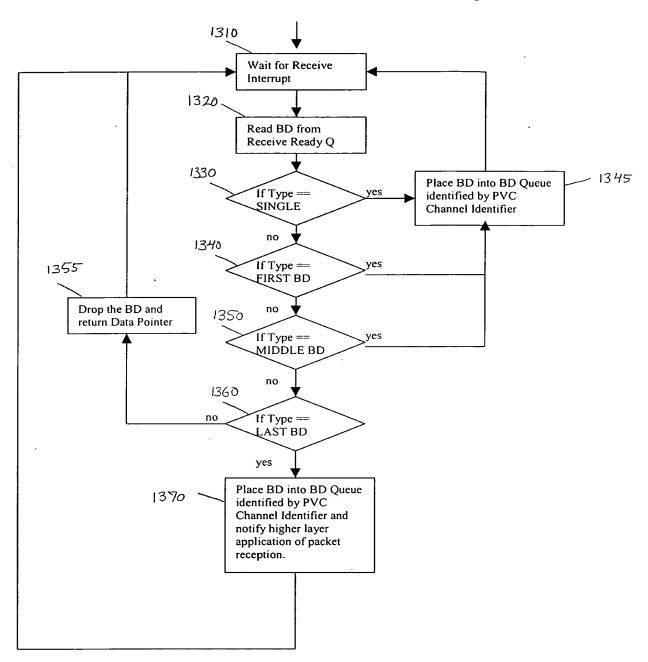
F1C7. 10



F1G.11



F16.12



F1G.13

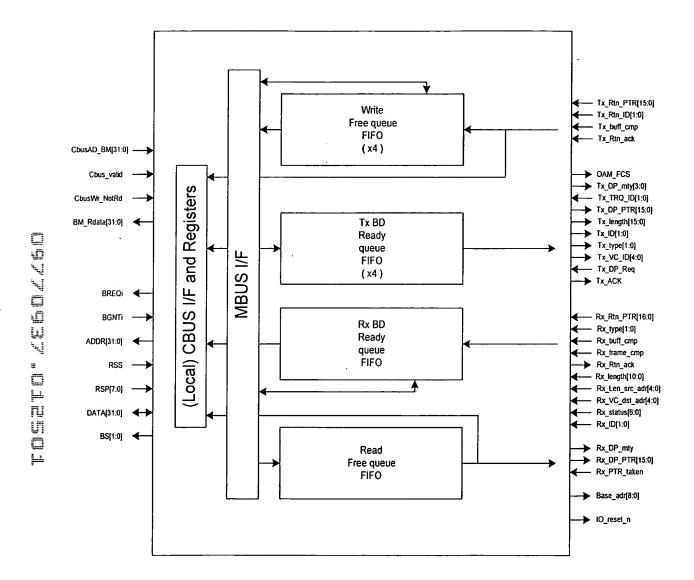


FIG. 14